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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,616	08/18/2003	Uwe Guenther	10191/3333	4950

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,616	GUENTHER, UWE	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-15* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/18/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Lee et al., US Patent no. 6,934,785 [Lee].

Regarding claim 1, AAPA discloses a method for a serial transmission of data between a processor module and at least one peripheral element, comprising:

transmitting a timing signal via two timing lines between the processor module and the at least one peripheral element [page 2, lines 15-20]; and

transmitting a data signal via two data lines between the processor module and the at least one peripheral element [page 2, lines 15-20].

AAPA does not disclose transmitting a selection signal via the two data lines. Lee discloses transmitting a selection signal via the data lines of a data bus [column 4, lines 16-21]. It would have been obvious to one of ordinary skill in the art to incorporate the Lee teachings into the AAPA method. Embedding selection signals into signals transmitted over a data bus removes the burden on other buses or signal lines of transmitting the selection signals.

Regarding claim 2, AAPA further discloses that the data signal is transmitted on a first data line and an inverted data signal is transmitted on a second data line [differential signals, page 2, lines 15-20].

Regarding claim 3, AAPA further discloses that the timing signal is transmitted on a first timing line and an inverted timing signal is transmitted on a second timing line [differential signals, page 2, lines 15-20].

Regarding claim 8, AAPA discloses a device for a processor module for serial transmission of data between the processor module and at least one peripheral element, comprising:

a first arrangement for transmitting a timing signal via two timing lines between the processor module and the at least one peripheral element [page 2, lines 15-20] and

a second arrangement for transmitting a data signal via two data lines between the processor module and the at least one peripheral element [page 2, lines 15-20].

AAPA does not disclose transmitting a selection signal via the two data lines. Lee discloses transmitting a selection signal via the data lines of a data bus [column 4, lines 16-21]. It would have been obvious to one of ordinary skill in the art to incorporate the Lee teachings into the AAPA device. Embedding selection signals into signals transmitted over a data bus removes the burden on other buses or signal lines of transmitting the selection signals.

Regarding claim 9, AAPA further discloses that the data signal is transmitted on a first data line and an inverted data signal is transmitted on a second data line [differential signals, page 2, lines 15-20].

Regarding claim 10, AAPA further discloses that the device is a serial-peripheral-interface-bus interface [page 1, lines 19-21].

Regarding claim 11, AAPA discloses a processor module, comprising:

a device for a serial transmission of data between the processor module and at least one peripheral element [page 1, lines 19-21];

wherein the device transmits a timing signal via two timing lines between the processor module and the at least one peripheral element [page 2, lines 15-20]; and

wherein the device transmits a data signal via two data lines between the processor module and the at least one peripheral element [page 2, lines 15-20].

AAPA does not disclose transmitting a selection signal via the two data lines. Lee discloses transmitting a selection signal via the data lines of a data bus [column 4, lines 16-21]. It would have been obvious to one of ordinary skill in the art to incorporate the Lee teachings into the AAPA device. Embedding selection signals into signals transmitted over a data bus removes the burden on other buses or signal lines of transmitting the selection signals.

Regarding claim 12, AAPA further discloses that the data signal is transmitted on a first data line and an inverted data signal is transmitted on a second data line [differential signals, page 2, lines 15-20].

Regarding claims 13-15, AAPA further discloses that the processor module is a control unit of a motor vehicle [page 1, lines 7-11].

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Lee et al., US Patent no. 6,934,785 [Lee], in view of, Coakeley et al., US Patent no. 6,920,604 [Coakeley].

Regarding claims 4 and 5, AAPA and Lee, as described above, disclose a method of transmitting selection signals on a differential serial data bus. AAPA and Lee are silent as to

how the selection signals are communicated over the differential data bus. Coakeley discloses using symmetry violations [parity violations] to communicate special information [data stream delineation] over a data bus while data is being transmitted over the bus [column 6, lines 6-18 and 55-59]. It would have been obvious to one of ordinary skill in the art to use symmetry violations in the AAPA and Lee method to transmit the selection signals over the differential data bus. One would be motivated to use symmetry violations to transmit the selection signals over the differential data bus to allow the selection signals to be transmitted at the same as normal data signals on the data bus [Coakeley, column 6, lines 55-60].

Allowable Subject Matter

Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Girzon et al., US Patent no. 6,378,017, discloses a bus with two clock lines and two data line for serial transmission of data between a processor and peripheral circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
June 23, 2006

JAMES K. TRUJILLO
PATENT EXAMINER
TC 2100